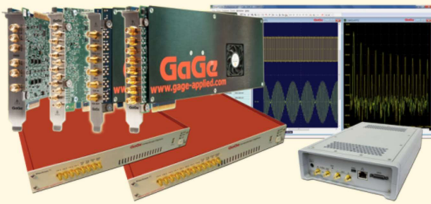


GaGe is a worldwide industry leader in high speed data acquisition solutions featuring a portfolio of the highest performance digitizers, PC oscilloscope software, powerful SDKs for custom application development, and turnkey integrated PC-based measurement systems.



APPLICATIONS

Wideband Signal Analysis
RADAR Design and Test
Signals Intelligence (SIGINT)
Ultrasonic Non-Destructive Testing
LIDAR Systems
Communications
Optical Coherence Tomography
Spectroscopy
High-Performance Imaging
Time of Flight
Life Sciences
Particle Physics

12-Bit PCIe Gen3 EON Express

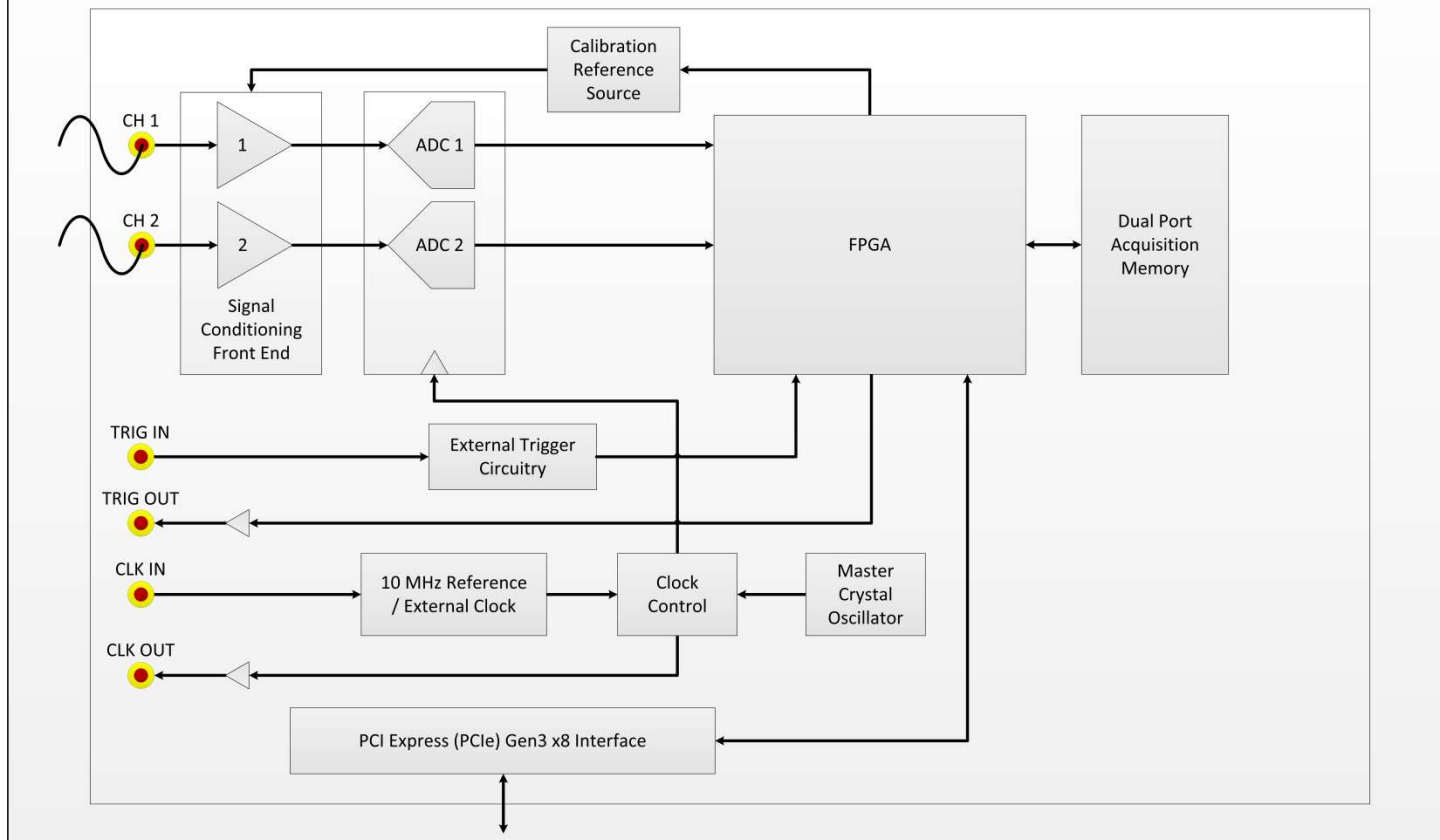
**Unprecedented Speed & Resolution in a 6 GS/s Streaming Digitizer
1.75 GHz Bandwidth with Stream Rates at 4+ GB/s**



FEATURES

- 12-Bit Vertical A/D Resolution with 2 or 1 Digitizing Input Channels
- 6 GS/s Maximum A/D Sampling Rate for 1 Digitizing Input Channel
- 3 GS/s Maximum A/D Sampling Rate for 2 Digitizing Input Channels
- 27 Software Selectable A/D Sampling Rates from 1 kS/s to 6 GS/s
- 1.75 GHz Analog Input Bandwidth with ± 0.5 dB Flatness to 1.25 GHz
- True Sustained 8+ ENOB Over Wide 1 GHz Signal Frequency Range
- 2 GS (4 GB) Onboard Sample Memory, Expandable to 4 GS (8 GB)
- FPGA Based Applications for Real-Time DSP Functions
- Dual Port Memory with Sustained PCIe Gen3 Data Streaming at 4+ GB/s
- Full-Featured Front-End with DC Coupling (AC Optional) and 50 Ω Inputs
- 6 Software Selectable Input Voltage Ranges from ± 100 mV to ± 5 V
- Ease of Integration with External or Reference Clock In & Clock Out
- External Trigger In & Trigger Out with Advanced Triggering Operations
- PCI Express (PCIe) Generation 3.0 x8 Interface Card
- Programming-Free Operation with GaGeScope PC Oscilloscope Software
- Software Development Kits Available for C/C#, LabVIEW and MATLAB
- Windows 10/8/7 and Linux Operating Systems Supported

EON Express CompuScope Simplified Block Diagram



Analog Input Front End

The EON Express is available in two models: a single channel model supporting a maximum A/D sampling rate up to 6 GS/s or a two channel model supporting a maximum A/D sampling rate up to 3 GS/s per channel. For the two channel model, ADC data can be captured in either dual channel or single channel mode.

The analog input bandwidth is 1.75 GHz with ± 0.5 dB flatness to 1.25 GHz for both models. The input channels are fixed for DC-coupling with fixed 50 Ω input impedance. Onboard auto-calibration provides DC accuracy of $\pm 0.5\%$. This wide 1.75 GHz bandwidth is especially useful for RF based applications by enabling direct RF sampling of wider band signals.

A configuration for fixed AC-coupling with fixed 50 Ω input impedance is available as an option. The coupling front end is factory hardware configured and is not software switchable. Note that it is also possible to externally implement AC-coupling with the use of an external high-pass filter. AC-coupling is useful for applications in which a small AC signal is sitting upon a large DC bias. In these cases, the DC bias can be removed with AC-coupling to reduce the input range for better signal fidelity.

All EON Express models feature six software selectable input voltage ranges of: ± 100 mV, ± 200 mV, ± 500 mV, ± 1 V, ± 2 V, and ± 5 V. These multiple input voltage ranges allow for optimal exploitation of the 12-bit ADC resolution to maximize dynamic parameter performance.

ADC Clock Circuit

The EON Express utilizes an onboard fixed master crystal oscillator as the primary internal clock source for the ADCs combined with clock control to effectively produce 27 software selectable A/D sampling rates ranging from 1 kS/s to 6 GS/s with a rate accuracy of ± 1 Part Per Million (PPM).

The ADC clock can also be supplied by an external clock input source, allowing for variable clock sample frequencies from 200 MHz to 3 GHz. External clock input signals are routed almost directly to the ADC chips so that each clock edge causes the ADC chips to produce exactly one sample. No re-clocking or Phase Lock Loop circuitry is used, since these methods may lead to extra or missing ADC clocks.

Use of an external clocking signal that is synchronous with the signal to be acquired achieves the best possible trigger stability with intrinsic jitter typically $\frac{1}{4}$ of a data point or better. Compared to using an internal clock source that is asynchronous (unrelated) to the signal trigger that can result in a 1 point trigger jitter between acquisitions.

When internally clocking, the ADC clocking signal is produced by a Voltage Controlled Crystal Oscillator (VCXO) within an on-board Phase Lock Loop (PLL) circuit. The PLL is disciplined by an on-board 10 MHz reference signal that has a frequency accuracy of order ± 1 PPM. This circuitry ensures that the frequency of the VCXO is reset every 100 nanoseconds so that the ADC sampling clock inherits the accuracy and stability of the 10 MHz reference input.

The ± 1 PPM internal sampling rate accuracy is sufficient for most digitizer applications. However some applications (notably communications), require ultra-high ADC clocking accuracy and stability. External atomic or IRIG sources can provide 10 MHz reference frequency accuracies and stabilities that are measured in Parts-Per-Billion. For these requirements, an external 10 MHz reference clocking signal source can be applied to the external clock input. Activating reference clocking from the controlling software will switch the PLL/VXCO input from the digitizer's 10 MHz reference signal to the supplied external 10 MHz reference signal. The ADC sampling will then inherit the accuracy and stability of the supplied external 10 MHz reference signal.

A clock output connector can be used to provide a clock out signal to serve as an external clocking source for other external devices. The clock out signal frequencies range from 200 MHz to 3 GHz, or can be configured to output the onboard 10 MHz reference signal.

Acquisition Memory

The EON Express includes 2 GS (4 GB) of onboard acquisition sample memory that can be optionally expanded to a maximum of 4 GS (8 GB). The onboard acquisition memory size is shared and equally divided among all active input channels (1 or 2) when acquiring data to onboard memory.

With the optional eXpert PCIe Data Streaming FPGA Firmware package, the dual-port architecture of the onboard memory is utilized as a large FIFO buffer for streaming acquired data to host PC memory via the digitizer's PCIe Gen3 x8 interface at sustained rates up to 4+ GB/s. This streaming mode can be effectively utilized to conduct real-time sustained host-based signal processing and/or signal recording operations of the acquired data.

Triggering

Advanced triggering operations include Simple, Complex, Windowed, and Multi-channel Boolean ORed.

Simple triggering uses a single trigger source from any input channel, external trigger, or software with software controls for trigger level and trigger slope (positive or negative). Each time the selected trigger source signal crosses the set trigger level with set trigger slope, a digital trigger is generated to initiate acquisition.

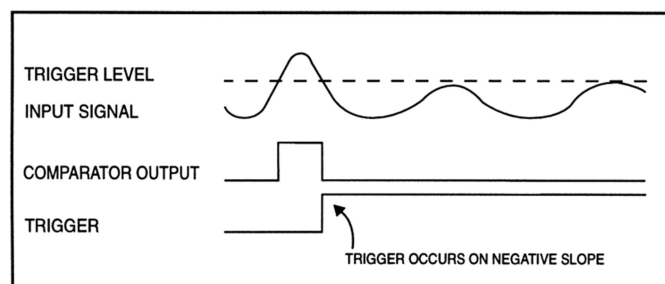


Figure: Generation of a Trigger Signal – Negative Slope

In order to avoid triggering on noise, the EON Express features a trigger sensitivity value of $\pm 5\%$ of Full Scale Input Range (FSIR) of the trigger source. This value specifies the minimum amount by which the trigger signal must swing through the trigger level in order to cause a trigger event.

An optional Trigger Timeout value can also be specified to establish the amount of time that the digitizer will wait for a trigger event before the driver forces a trigger event to occur.

Complex triggering makes use of multiple trigger engines and their configurations. Trigger configurations for each logical triggering engine require three specifications: the engine's source, the engine's trigger level and the engine's trigger conditions. The outputs of each logical triggering engine are Boolean ORed together to create the overall triggering signal. There are two trigger engines for each input channel plus one trigger engine for the external trigger input. Usage of complex triggering allows for Windowed Triggering and Multi-channel Boolean ORed triggering.

Windowed Triggering uses two trigger engines in such a way that a trigger event occurs if the signal voltage leaves a range of voltages specified by an upper limit and a lower limit. Windowed triggering is implemented by selecting the same input channel as the trigger source for two trigger engines.

The levels for the two engines are then selected as the upper and lower limit with positive and negative slopes, respectively. In this way, if the signal voltage rises above the upper limit, the first engine triggers and if the signal voltage falls below the lower limit, the second engine triggers.

Since the outputs of both trigger engines are Boolean ORED together, a trigger on either engine will cause a global trigger event to occur.

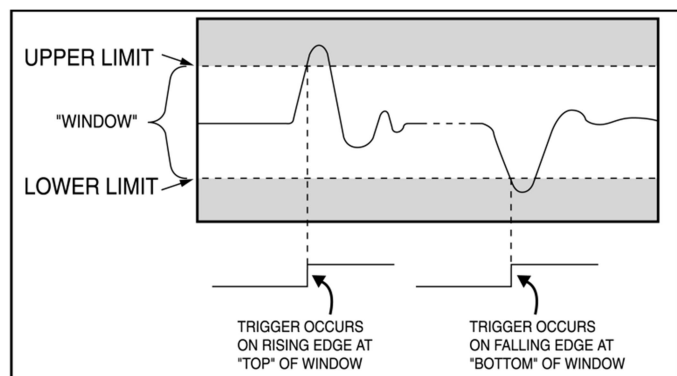


Figure: Windowed Triggering

Multiple Record Mode

Multiple Record Mode uses the digitizer onboard memory to allow ultra-rapid repetitive waveform acquisition. In Multiple Record Mode, sequentially acquired waveforms are stacked in onboard memory, so that data transfer to host PC RAM is not required between waveforms. Furthermore, in Multiple Record Mode, re-arming of trigger circuitry is done in hardware with no software intervention required.

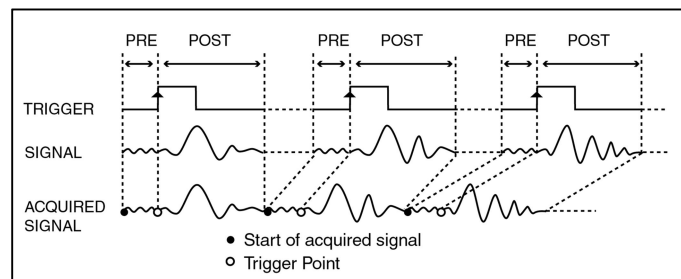


Figure: Multiple Record Mode with Pre-Trigger Data

Pre-trigger data can also be captured in Multiple Record Mode. Memory usage is well optimized in Multiple Record Mode since only the small amount of pre- and post-trigger data containing the pulse of interest are stored to memory. Memory is not wasted in the acquisition of the entire signal between pulses, which is not of interest.

Timestamping

Timestamping is a feature used to determine the arrival time of waveform trigger events and is most useful when used in Multiple Record Mode. The digitizer has a 44-bit on-board numerical counter. The clock source for the counter may be selected as the digitizer sampling clock or a fixed on-board clock source. The value of the timestamp counter can be reset to zero at the beginning of each acquisition sequence or can be alternatively reset from software at some referenced time.

During an acquisition and upon each trigger event, the current output value of the timestamping counter is latched and is stored in onboard memory as a footer to the current record. After acquisition, the timestamp value associated with each acquired record may be downloaded. When dividing the timestamp value by the known counter source frequency, the occurrence time of each trigger event is obtained.

PCI Express (PCIe) Generation 3 x8 Interface

The EON Express utilizes a PCIe Gen3 x8 (8-lane) interface to the host PC and thus requires an open available physical PCIe x8 or larger x16 size slot on the host PC system for installation.



The EON Express is fully backwards compatible with previous PCIe Gen2 and Gen1 based slots. It is also possible to operate the EON Express in PCIe slots that are physically x8 or x16 in size but electrically operate at slower x1 or x4 PCIe speeds.

For maximum data transfer rate performance, it is best to install the EON Express in a dedicated (non-switched) PCIe Gen3 x8 or larger PCIe Gen3 x16 slot. The host system should provide good cooling air flow for the installed EON Express card location with ideally an empty adjacent slot to prevent blockage of the card's onboard cooling fan.

With the optional eXpert PCIe Data Streaming FPGA Firmware package, acquired data can be streamed to host PC memory via the PCIe Gen3 x8 interface at real-time sustained rates up to 4+ GB/s for targeted host-based signal processing and/or signal recording operations.

Multi-Card Systems

Multiple EON Express cards can work together either within a single system or across multiple systems in three possible configurations: Independent, Synchronized Cascade, or Synchronized Split.

In an Independent configuration, each card simply operates independently within the system.

In a Synchronized Cascade configuration, each card operates together as a group by cascading the trigger signal via the Trigger Out. The Clock Out can be similarly cascaded if synchronous clocking is required. This mode has a small constant delay between each channel but requires no external clocking source or RF splitters.

In a Synchronized Split configuration, each card operates together as a group by splitting the trigger signal to each card's Trigger In using an RF power splitter (not a BNC Tee) and same equal length cables. This can also be done with the External Clock input if synchronous clocking is required. This mode requires more external hardware but provides the best simultaneity between multiple cards.

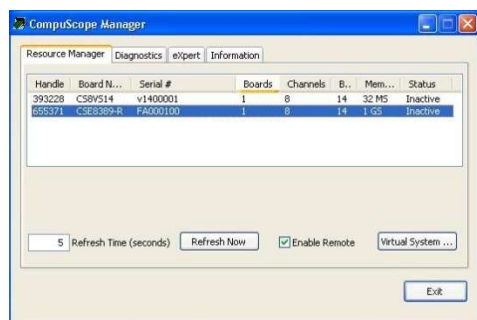
Application Software

The EON Express is supplied with 64-bit/32-bit device drivers supporting Windows 10/8/7 and Linux distributions for Red Hat and Ubuntu. Note that other Linux distributions can be supported as well.

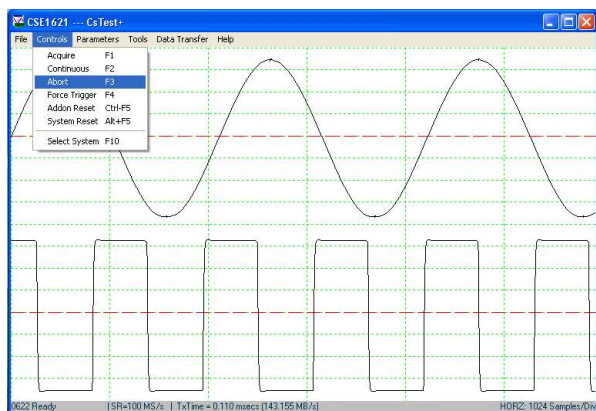
For Linux, device drivers, C Application Programming Interface (API), and C Software Development Kit (SDK) examples are included.

For Windows, a CompuScope Manager Utility, CTest+ Utility and the GaGeScope Lite Edition application is included:

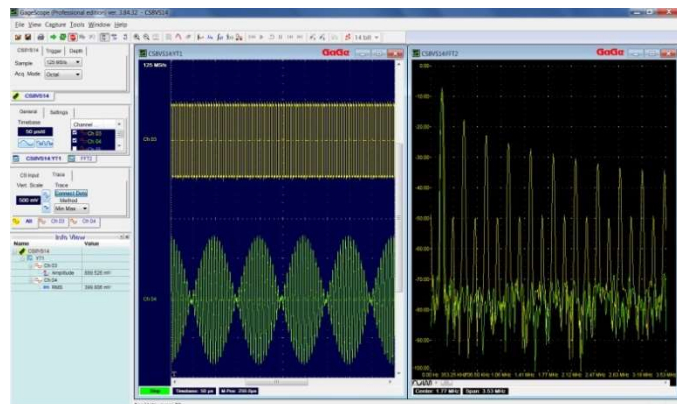
The CompuScope Manager Utility is used to enable and verify certain hardware configurations of the digitizer and provides details on resource usage, diagnostics, eXpert features, and hardware/software/firmware versioning information.



The CTest+ Utility is a simple application to conduct basic capture of signals and to verify basic correct operation of the digitizer card.



The included and more advanced GaGeScope Lite Edition is a solutions oriented PC oscilloscope application that allows users to quickly and easily control the digitizers without having to write a single line of code. Data can be displayed, analyzed, printed and saved with an easy-to-use Windows-based user interface.



Optional upgrades to the Standard or Professional versions of GaGeScope provide access to more advanced features and functionalities.

Software Development Kits

GaGe provides extensive software for custom application development with optional Software Development Kits (SDKs) for C/C#, MATLAB, and LabVIEW. All SDKs provide several powerful programming examples illustrating the use of the digitizer hardware in different operating modes. These sample programs serve as a starting point for users to develop customized software applications optimized for their specific application requirements.

eXpert FPGA Processing Firmware Options

The default EON Express configuration can store raw acquired waveform data and transfer them quickly to the user for analysis, display and/or storage.

The addition of optional eXpert FPGA processing firmware features allow for some signal processing analysis to be performed on the digitizer hardware itself within its onboard Field Programmable Gate Array (FPGA).

There are three primary advantages to the processing of waveform data using an eXpert firmware option. First, data can be processed at full sampling rate speeds, where data rates may exceed what can be sustained for streaming over the PCIe bus to other targeted processing devices. Second, processing data onboard the digitizer hardware reduces the data processing load on the host computer. Third, onboard processing may provide data reduction that reduces the data transfer traffic on the host bus and allow for a greater raw data acquisition rate.

eXpert FPGA feature packages are loaded from an onboard flash memory module and are designed to be transparent to the standard digitizer drivers for Windows/Linux. Only one eXpert FPGA feature can be utilized at a time.

eXpert FPGA feature packages can be purchased at any time and can be implemented on digitizers already in use in the field by existing customers without requiring the digitizer to be returned to GaGe for reprogramming.

GaGe can also develop customized firmware to meet specific customer application requirements. Please contact us with a summarized listing of application requirements to evaluate for design feasibility. Pricing for customized FPGA development is highly dependent on the scope of the project work and on expected product volume.

Current eXpert FPGA features available for the EON Express include:

eXpert FPGA Feature	Feature Description
PCIe Data Streaming	Allows for data streaming mode of acquired data directly through the PCIe interface to the host PC RAM and on to targeted host based CPU or dedicated processing cards for analysis and/or to high-speed storage systems for real-time signal recordings.
Signal Averaging	Allows for detection of very small repetitive signals in a noisy environment. Using rapid signal averaging, small signals can be extracted from a background of high amplitude noise, which may even be larger than the actual signal itself.
Optical Coherence Tomography (OCT)	Supports variable rate k-clocking or inactive external clock by simultaneously digitizing the interferometer signal with the returned optical signal for use with OCT applications.
Fast Fourier Transform (FFT)	Allows 512, 1024, or 2048 point FFT calculation analysis directly on the digitizer and transfer of multiple Fourier Spectra to the host PC in a single PCIe transfer.
Digital Down Conversion (DDC)	Digitally down convert higher frequencies with various decimation factors for a targeted specified NCO frequency with included PCIe data streaming capability to effectively record only the data of interest.

Sig-Station System Options



Optional Sig-Stations are available for providing complete turn-key systems for the EON Express. Sig-Stations are high-performance PC workstations that are designed specifically for integrating GaGe advanced instruments and maximizing their operational performance.

Sig-Stations come with all GaGe cards, features, and software fully tested and installed so that the user can be up and running with their system solution right out of the box; thus saving time and minimizing risks of self-integrated systems. Custom system configurations can be defined to meet specific customer application requirements.

These systems incorporate the latest in PC-based technology and utilize workstation class motherboards with multiple dedicated bandwidth PCIe slots, high multi-core count Xeon CPUs, and large system memory capacity. Integrated high-speed data storage systems for real-time signal recording applications requiring a guaranteed continuous sustained data streaming rate with no missing data can be included.

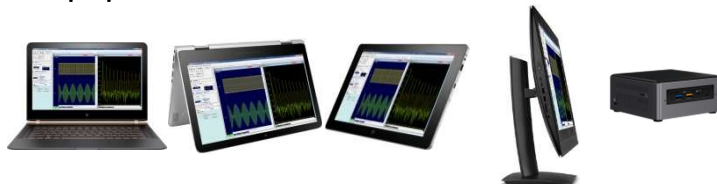
Contact us to configure a system tailored for your application.

Thunderbolt 3 Options

Utilize the EON Express via the Thunderbolt 3 interface for PC system device form factors with either limited or no PCIe expansion slots such as:



Laptops 2-in-1s Tablets All-in-Ones Mini PCs



In Thunderbolt 3 mode, up to four lanes of PCIe Gen3 is supported for a maximum rate of 32 Gbps (4 GB/s); making it an ideal match for optimal data transfer performance of the EON Express PCIe Gen3 Digitizer to connected PC devices.

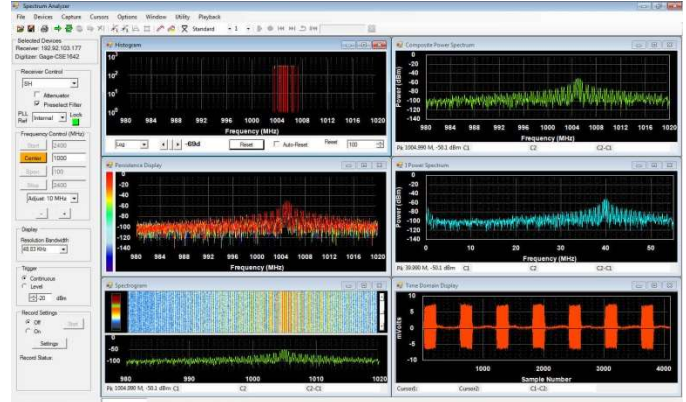
Wideband RF Signal Analyzer Recorders

The EON Express can be combined with wideband downconverters and PC solutions to be the heart of a wideband, multi-channel, RF/Microwave signal analysis and recording system covering signal frequencies up to 40 GHz with 500 MHz bandwidth at 1 GHz IF.



The 2-channel EON Express model can support 1 receiver with a wideband mode of 500 MHz BW and narrower band modes of either 100 MHz or 50 MHz BW. 10 MHz reference inputs and outputs on both the digitizers and receivers provide a single frequency reference for synchronized system performance.

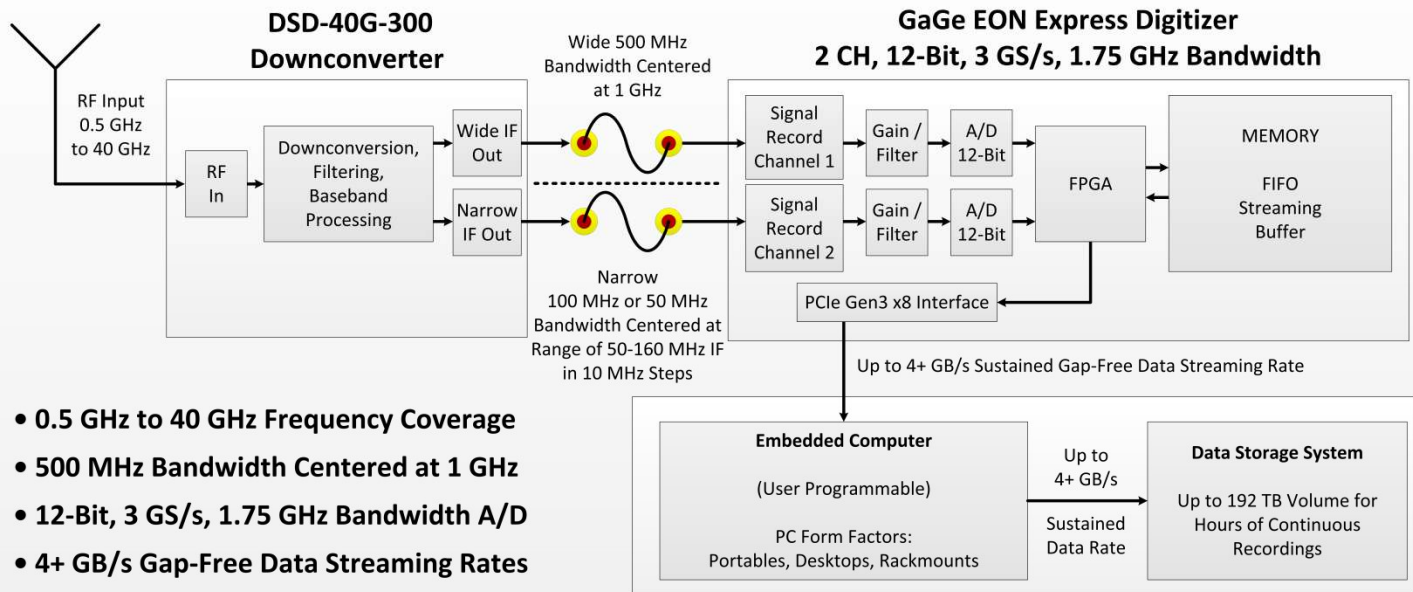
The spectrum analyzer software, SpectraScopeRT, requires no programming and allows for control of receiver center frequency, bandwidth, and signal recordings. SpectraScopeRT features real-time FFT power spectrums (with peak hold and persistence), spectrograms, histograms, and time domain displays while recording, and upon recording playback.



SpectraScopeRT also supports dual receiver, double bandwidth operation for both real-time display and gap-free recording. This allows 2 downconverters feeding digitizers to display and record parallel side by side bandwidths, effectively doubling the available bandwidth, up to 1 GHz.

The digitizers and receivers have full control and data acquisition support via Mathworks MATLAB, with example programs furnished to facilitate rapid signal processing and modulation analysis program development. Additional SDKs and example programs are provided for C/C# and LabVIEW.

500 MHz Bandwidth 12-Bit Signal Analyzer System



- 0.5 GHz to 40 GHz Frequency Coverage
- 500 MHz Bandwidth Centered at 1 GHz
- 12-Bit, 3 GS/s, 1.75 GHz Bandwidth A/D
- 4+ GB/s Gap-Free Data Streaming Rates

MAIN SPECIFICATIONS

Model #	:	CSE123G2	CSE126G1
# of Input Channels	:	2	1
Max. Rate per Channel	:	3 GS/s	6 GS/s
Vertical A/D Resolution	:	12-bits	12-bits

ANALOG INPUT CHANNELS

Connectors	:	SMA
Impedance	:	50 Ω
Coupling	:	DC (standard) or AC (option)
Analog Bandwidth	:	1.75 GHz
Flatness	:	Within ± 0.5 dB of ideal response to 1.25 GHz
Voltage Ranges (software selectable)	:	± 100 mV, ± 200 mV, ± 500 mV, ± 1 V, ± 2 V, ± 5 V
DC User Offset (software selectable)	:	Spans Full Scale Input Range (FSIR)
DC Accuracy	:	$\pm 0.5\%$
Absolute Max. Input	:	± 6 V (over-voltage protection included)
Interchannel Skew	:	< 50 picoseconds
Interchannel Skew Jitter	:	< 3 picoseconds RMA

A/D SAMPLING

Rates per Channel (software selectable)	:	6 GS/s, 3 GS/s, 1.5 GS/s, 1 GS/s, 750 MS/s, 500 MS/s, 375 MS/s, 250 MS/s, 187.5 MS/s, 125 MS/s, 75 MS/s, 50 MS/s, 30 MS/s, 20 MS/s, 10 MS/s, 4 MS/s, 2 MS/s, 1 MS/s, 500 kS/s, 200 kS/s, 100 kS/s, 50 kS/s, 20 kS/s, 10 kS/s, 5 kS/s, 2 kS/s, 1 kS/s
Rate Accuracy	:	± 1 part-per-million (0° to 50° C ambient)

ACQUISITION MEMORY

Acquisition memory size is shared and equally divided among all active input channels (1 or 2).

Standard Size	:	2 GS (4 GB)
Optional Sizes	:	4 GS (8 GB)
Architecture	:	Dual Port
Data Streaming	:	Yes

Performance

The EON Express features an incredibly flat frequency response over its entire 1.75 GHz input bandwidth with shown ± 0.5 dB flatness up to 1.25 GHz.

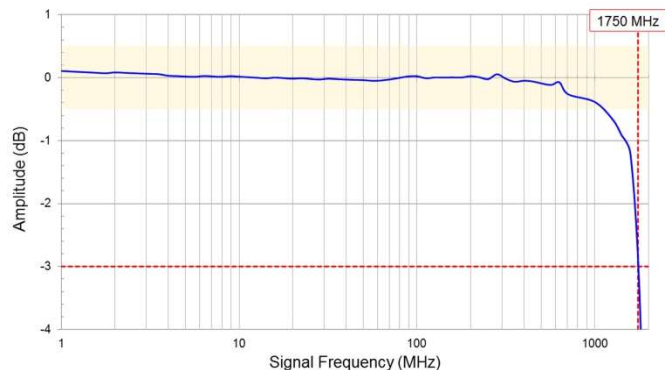


Figure: EON Express Frequency Response Curve
Sampling Rate 3 GS/s, ± 500 mV, DC Coupling, 50 Ω

GaGe high-performance digitizers are also renowned for sustaining the maximum effective number of bits (ENOB) over a wide signal frequency range with quality signal conditioning and signal fidelity features.

Note the stable consistency of ENOB and dynamic parameter performance for the EON Express over the extremely wide signal frequency range values up to 1 GHz!

± 500 mV, DC Coupled, 50 Ω , Sampling Rate 3 GS/s						
Signal Frequency	10 MHz	70 MHz	100 MHz	199 MHz	500 MHz	1 GHz
ENOB	8.9 Bits	8.8 Bits	8.8 Bits	8.7 Bits	8.2 Bits	8.0 Bits
SNR	55.3 dB	54.9 dB	54.9 dB	54.3 dB	55.6 dB	51.5 dB
THD	-71.5 dB	-64.4 dB	-63.4 dB	-63.5 dB	-52.1 dB	-54.0 dB
SINAD	55.2 dB	54.5 dB	54.5 dB	53.9 dB	50.8 dB	49.6 dB
SFDR	71.1 dB	70.0 dB	70.8 dB	70.6 dB	71.4 dB	69.6 dB

± 200 mV, DC Coupled, 50 Ω , Sampling Rate 3 GS/s						
Signal Frequency	10 MHz	70 MHz	100 MHz	199 MHz	500 MHz	1 GHz
ENOB	8.6 Bits	8.6 Bits	8.4 Bits	8.4 Bits	8.1 Bits	7.8 Bits
SNR	53.5 dB	53.5 dB	52.4 dB	52.8 dB	52.8 dB	50.3 dB
THD	-67.9 dB	-65.6 dB	-63.5 dB	-64.0 dB	-53.9 dB	-53.0 dB
SINAD	53.3 dB	53.3 dB	52.2 dB	52.5 dB	50.4 dB	48.4 dB
SFDR	70.7 dB	71.1 dB	69.6 dB	70.0 dB	70.8 dB	70.2 dB

± 100 mV, DC Coupled, 50 Ω , Sampling Rate 3 GS/s						
Signal Frequency	10 MHz	70 MHz	100 MHz	199 MHz	500 MHz	1 GHz
ENOB	8.0 Bits	8.0 Bits	7.8 Bits	7.8 Bits	7.8 Bits	7.4 Bits
SNR	50.0 dB	49.8 dB	48.8 dB	49.2 dB	49.3 dB	47.8 dB
THD	-66.9 dB	-64.6 dB	-59.4 dB	-61.6 dB	-55.6 dB	-52.0 dB
SINAD	49.9 dB	49.7 dB	48.6 dB	48.8 dB	48.5 dB	46.4 dB
SFDR	71.5 dB	69.6 dB	70.8 dB	70.6 dB	71.3 dB	70.0 dB

TRIGGERING

Engines	:	2 per Channel, 1 for External Trigger
Source	:	Any Input Channel, External Trigger or Software
Input Combination	:	All Combinations of Sources Logically OR'ed
Slope	:	Positive or Negative (software selectable)
Sensitivity ¹	:	±5% of Full Scale Input Range of Trigger Source

EXTERNAL TRIGGER

Connector	:	SMA
Impedance	:	≈ 1k Ω
Coupling	:	AC
Bandwidth	:	>100 MHz
Voltage Range	:	0-3 V (unipolar)

TRIGGER OUT

Connector	:	SMA
Impedance	:	50 Ω
Amplitude	:	0 – TTL

CLOCK IN

Connector	:	SMA
Signal Level	:	Minimum 0.2 V RMS, Maximum 0.5 V RMS
Impedance	:	50 Ω
Coupling	:	DC
Duty Cycle	:	50% ±5%
Input Modes	:	External Clock or 10 MHz Reference Clock
External Clock Mode Rates	:	Minimum 200 MHz, Maximum 3 GHz
Variable/Inactive External Clock Mode	:	Supports variable rate k-clocking or inactive external clock, particularly useful for OCT applications.

CLOCK OUT

Connector	:	SMA
Signal Level	:	0 – 1.5 V
Impedance	:	50 Ω Compatible
Duty Cycle	:	50%
Output Modes	:	Half Sampling Clock Frequency or 10 MHz Reference Clock
Sampling Clock Mode Rates	:	Minimum 200 MHz, Maximum 3 GHz
10 MHz Reference Clock Mode Rate	:	10 MHz (from External Clock)

MULTIPLE RECORD

Pre-Trigger Data	:	Up to FPGA Memory Size
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TIME-STAMPING

Timing Resolution	:	One Sample Clock Cycle
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MULTI-CARD SYSTEMS

Independent	:	Each card operates independently within the system.
Synchronized Cascade	:	Each card operates together as a group by cascading the trigger signal via the Trigger Out. The Clock Out can be similarly cascaded if synchronous clocking is required. This mode has a small constant delay between each channel but requires no external clocking source or RF splitters.
Synchronized Split	:	Each card operates together as a group by splitting the trigger signal to each card's Trigger In using an RF power splitter (not a BNC Tee) and same equal length cables. This can also be done with the External Clock input if synchronous clocking is required. This mode requires more external hardware but provides the best simultaneity between multiple cards.

DIMENSIONS

Size	:	Single Slot PCIe, Full Height, 10.1 in (256.54 mm) Length
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POWER CONSUMPTION

Power	:	25 Watts (typical)
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PC SYSTEM REQUIREMENTS

PCI Express (PCIe) Slot	:	1 Free Full-Height PCIe x8 or x16 Gen3, Gen2 or Gen1 Slot.
Host System Cooling	:	Provide good cooling air flow for installed EON Express location with ideally an empty adjacent slot to prevent blockage of card's onboard cooling fan.
Operating System	:	Windows 10/8/7 (64-bit/32-bit) Linux – Requires SDK for C/C# – for Red Hat or Ubuntu (Note that other Linux distributions can be supported as well.)

¹ Signal amplitude must be at least 10% of Full Scale Input Range of Trigger Source to cause a trigger event. Smaller signals are rejected as noise.

ORDERING INFORMATION

Hardware

Model Number	A/D Resolution	# of Channels	Max. Sampling Rate per Channel	Input Bandwidth	Memory Size	Order Part Number
CSE123G2	12-Bit	2	3 GS/s	1.75 GHz	2 GS (4 GB)	ENE-123-G20
CSE126G1	12-Bit	1	6 GS/s	1.75 GHz	2 GS (4 GB)	ENE-126-G10

Memory Upgrades

Memory Upgrade: 4 GS (8 GB)	ENE-181-001
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Front End Options

AC-Coupled Front End Option (Hardware configured at factory.)	ENE-FAC-001
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Cable Accessories

Set 1 Cable SMA to BNC	ACC-001-031
Set 4 Cable SMA to BNC	ACC-001-033

eXpert FPGA Firmware Options

eXpert PCIe Data Streaming	STR-181-000
eXpert Signal Averaging	250-181-001
eXpert Fast Fourier Transform (FFT)	250-181-004
eXpert Digital Down Conversion (DDC)	250-181-005
eXpert Optical Coherence Tomography (OCT)	250-181-006

GaGeScope Software

GaGeScope: Lite Edition	Included
GaGeScope: Standard Edition	300-100-351
GaGeScope: Professional Edition	300-100-354

Software Development Kits (SDKs)

GaGe SDK Pack (includes C/C#, MATLAB, LabVIEW SDKs)	200-113-000
CompuScope SDK for C/C#	200-200-101
CompuScope SDK for MATLAB	200-200-102
CompuScope SDK for LabVIEW	200-200-103

WARRANTY

Standard two years parts and labor.

Unless otherwise specified, all dynamic performance specs have been qualified on engineering boards. All specifications subject to change without notice.

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